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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,364	11/13/2001	Miaochen Wu	3070.1010-000	4380

28120 7590 03/08/2005

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EXAMINER	
JOSEPH, JAISON	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,364	WU, MIAOCHEN	
	Examiner	Art Unit	
	Jaison Joseph	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 6 and 12 are objected to because of the following informalities: Claim 6 line 3 recites "200 mili Volts" should have been "200 milli Volts". Appropriate correction is required.

Similar scenarios found in claim 12, line 3 . Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duggan et al. (6,359,942) in view of Lee et al (6,014,768).

Regarding claim 1, Duggan et al. teach a slicer with threshold voltage circuit generating plurality of threshold signals N1, N2 and N3, and comparator 39, 40, and 41 (see figure 5). Duggan et al. failed to teach a differential comparator with a first differential amplifier and a second differential amplifier, the first and second differential amplifiers cross-coupled to output a signal depend on a the inputs coupled to the first differential amplifier and the second differential amplifier. However, Lee et al teach a differential comparator in figure 8A with a first differential amplifier (components 804, 805, 808, 813, 814, 815, 816, and 821) and second differential amplifier (components

803, 804, 809, 813, 814, 817, 818, and 822), the first and the second differential amplifiers cross-coupled (via line 830 and 831) to output a signal depend on a the inputs coupled to the first differential amplifier and the second differential amplifier (C1 and C1B). Therefore, it would be obvious to an ordinary skilled in the art at the time the invention was made to Lee et al.'s differential comparator in Duggan et al.'s slicer to generate an ideal waveform that tracks the input signal.

Regarding claim 2, which inherits the limitations of claim 1, Duggan et al further discloses the slicer having plurality of comparators (see figure 5. components 39, 40, and 41)

Regarding claim 3, which inherits the limitations of claim 1, Lee et al further teach in figure 8A a non-inverting input of the first differential amplifier is coupled to a first transistor 804 and an inverting input of the first differential amplifier is coupled to a second transistor 805, a non-inverting input of the second differential amplifier is coupled to a third transistor 804 and an inverting input of the first differential amplifier is coupled to a second transistor 803. The first and second differential amplifiers cross-coupled by coupling collectors of the first transistor to the collector of the third transistor and coupling the collector of the second transistor to the collector of the fourth transistor (see column 13, lines 25 – 26).

Regarding claim 4, which inherits the limitations of claim 1, Lee et al further teach a first emitter follower coupled to the first differential amplifier and a second emitter follower coupled to the second differential amplifier where the differential output coupled between the first emitter follower and the second emitter follower.

Regarding claim 5, which inherits the limitations of claim 2, Lee et al. teach the transistors are Bipolar Junction Transistors (see figure 8A). It is inherent to an ordinary skilled in the art that the transistors are used in linear region to benefit reduced distortion and to achieve accurate outputs.

Regarding claim 6, which inherits the limitations of claim 1, Duggan et al. failed tot teach the differential input signal is 600 milli volts peak to peak and the differential threshold signals are 200 milli volts, -200 milli volts and 0 volts. Lee et al teach detecting three different thresholds with a signal which peak-to-peak 2 volts (see figure 3). Lee et al. do not specifically disclose the peak to peak voltage is 600 millivolts and the thresholds are 200mV, -200mV, and 0 V. it is inherent in the art that different transistors operate in different voltage range. It would be obvious to an ordinary skilled in the art to use a voltage within the operating range of the transistor to function the transistors as a slicer.

Regarding claim 7, which inherits the limitations of claim 2, Duggan et al further teach a slicer with three comparators (see figure 5, components 39, 40 and 41).

Regarding claim 8, claimed method including the features corresponding to subject matter mentioned above rejection of claim 1 is applicable hereto.

Regarding claim 9, which inherits the limitations of claim 8, the claimed method including the features corresponding to subject matter mentioned above rejection of claim 3 is applicable hereto.

Regarding claim 10, which inherits the limitations of claim 8, claimed method including the features corresponding to subject matter mentioned above rejection of claim 4 is applicable hereto.

Regarding claim 11, which inherits the limitations of claim 9, claimed method including the features corresponding to subject matter mentioned above rejection of claim 5 is applicable hereto.

Regarding claim 12, which inherits the limitations of claim 8, claimed method including the features corresponding to subject matter mentioned above rejection of claim 6 is applicable hereto.

Regarding claim 13, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 1 is applicable hereto.

Regarding claim 14, which inherits the limitations of claim 13, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 3 is applicable hereto.

Regarding claim 15, which inherits the limitations of claim 13, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 4 is applicable hereto.

Regarding claim 16, which inherits the limitations of claim 15, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 5 is applicable hereto.

Regarding claim 17, which inherits the limitations of claim 13, claimed apparatus including the features corresponding to subject matter mentioned above rejection of claim 6 is applicable hereto.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jaison Joseph
02/25/2005

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